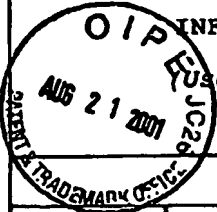
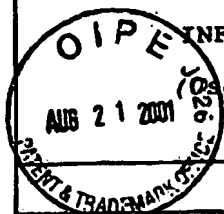


FORM PTO1449 (REV. 8-83)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 11587-M-10187-43C US	SERIAL NO. 09/867,836		
 <p>INFORMATION DISCLOSURE STATEMENT</p> <p>Use several sheets if necessary)</p>				APPLICANT Eliyahou Harari et al.			
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U. S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
AT	A12	4 3 9 3 4 7 5	07/1983	Kitagawa et al.			
AT	A13	4 4 1 5 9 9 2	11/1983	Adlhoch			
AT	A14	4 4 9 5 6 0 2	01/1985	Sheppard			
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)							
AT	C13	Torelli et al., "Non-Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-29, No. 3, pp. 103-13 (Aug. 1983)					
	C14	Excerpts from a 1983 Data Book published by SGS-ATES Group, 45 pp. (Nov. 1983)					
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	C16	Klingman, "Microprocessor Systems Design," <u>Prentice-Hall, Inc.</u> , pp. 30-31 (1977)					
	C17	Masuoka et al., "A 256-kbit Flash E ² PROM Using Triple-Polysilicon Technology," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 4, (August 1987)					
	C18	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987)					
AT	C19	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)					
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<p>* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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AT	A17 4 9 9 9 8 1 3	02/1991	Ohtsuka et al.			

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AT	C20	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 7A, pps. 3311-3314 (December 1981)

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